

REMARKS

Claims 16-20 and 31-45 are pending in the Application. Previously withdrawn Claims 1-15 and 21-30 have been canceled without prejudice. In the Office Action mailed February 23, 2007, Claims 16, 17 and 20 are rejected under 35 USC §102(b) as being anticipated by U.S. Patent 6,112,297 to Ray et al. ("Ray"). Claims 18 and 19 are rejected under 35 USC §103(a) as being unpatentable over Ray in view of U.S. Patent 5,517,627 to Peterson.

In response to the rejection of the claims as being anticipated by Ray, Applicants have amended independent Claim 16 to include steps of:

generating an input alignment signal indicating a
shift required to realign said plurality of input bytes;
configuring hardware according to a shifting
configuration based upon said input alignment signal to
selectively transfer input data;
realigning said input data in the hardware based
upon said shifting configuration

Support for the amendments may be found at least in Figs. 17 and 21, and the text of paragraphs [0042]-[0048] and [0053]. Applicants respectfully submit that the claims as amended clearly distinguish over Ray. Ray is directed to a method of processing misaligned load instructions. In particular, Ray teaches that when a load instruction is misaligned, two "primitive" instructions LD1 and LD2 are generated. The first instruction LD1 includes a 2-bit indicator identifying it as the first part of an instruction and is stored in a merge latch until the second instruction LD2 is detected. The instruction LD2 includes a 2-bit indicator identifying it as the final part of the instruction. After the instruction LD2 is received, both instructions are provided to a multiplexer to reassemble the instruction. (Col. 7, lines 2-38). Accordingly, Ray teaches storing bits associated with portions of an instruction which are misaligned to indicate which portion is first and which portion is second. In contrast, Claim 16 as amended includes a step of generating an input alignment signal indicating a shift required to align the plurality of input bytes. Applicants have also amended Claim 16 to indicate that configuring hardware comprises configuring hardware according to a shifting configuration based upon the input alignment signal, and that realigning the

input data is based upon the shifting configuration. Applicants respectfully submit that Ray fails to disclose or suggest generating an input alignment signal indicating a shift required to align the plurality of input bytes, or configuring hardware according to a shifting configuration based upon the input alignment signal as set forth in the amended claim. Applicants submit that the claims as amended distinguish over Ray, and respectfully requests reconsideration of the rejection of the claims in view of Ray.

In response to the rejection of the Claims 18 and 19 over Ray and Peterson, Applicants respectfully submit that Claims 18 and 19 are allowable over the combination of Ray and Peterson for the same reasons that Claim 16 as amended is allowable over Ray. Peterson also fails to disclose or suggest configuring hardware according to a shifting configuration based upon said input alignment signal to selectively transfer input data; or realigning said input data in the hardware based upon said shifting configuration.

Applicants have added new Claims 31-45. Support for the new claims may be also found in Figs. 17 and 21, and the text of paragraphs [0042]-[0048] and [0053]. All of the pending claims are directed to a method of realigning data of Group III, and are all based upon a single embodiment disclosed in Applicants' specification. Applicants submit that the new claims also distinguish over the cited references.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested. If there are any questions, the Applicants' attorney can be reached at Tel: 408-879-7710.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on May 2, 2007.

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Signature